# SEMICONDUCTOR CHIP

## ABSTRACT OF THE DISCLOSURE

A semiconductor chip able to reduce wasteful power loss due to a margin of power supply voltage considering variation of characteristics. A voltage setting signal for setting the power supply voltage to be supplied to a target circuit is generated in a voltage controller in the semiconductor chip based on a delay time of a delay signal of a replica circuit with respect to a clock signal. The maximum value of power supply voltage set by the voltage setting signal is restricted to the maximum value of the power supply voltage determined based on variations in production of the semiconductor chip. Accordingly, even when the value of the power supply voltage set based on the delay signal exceeds the maximum value due to the margin set considering the variation of characteristics, the voltage setting of the voltage setting signal output to the external power supply is restricted to the maximum value, so wasteful power loss can be suppressed.